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V1.04

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1.04

2020/09/17

0.90		ſ
0.91		ſ
1.00		ſ
1.01	1) 3.2.3 convertToIntegerExact ň roundToIntegralExact ſ 2) CSR	ſ
	1) 2.2.3 ɻ 2.2.5.1 ɻ 3.2.5 ſ	
	1)	
1.02		

	PC ┌ 2) 2.1.5 ┌ 3) 2.2.1.10 MULH.WU U ┌ 4) 3.1.4.4 2Emin Emin ┌ 5) 3.2.4.6 MOVCF2FR 3.2.4.7 MOVCF2GR 0 0 0 ┌ 6) 3.2.6.1 32 ┌ 7) 4.2.3.3 4.2.3.4 TLB CSR.TLBIDX.NE 1 TLB TLB ┌ 8) 5.2.1 ┌ 9) 5.4.3.4 ņINVTLB r0, r0 ņ ņINVTLB 0, r0, r0 ņ ┌ 10) 5.4.4 found_ppn ┌ 11) 6.2.2 ┌ 12) 7.4.1 7-2 DATF DATM ņ ň ň ň ň ņ ņ ň ň ň ň ņ ┌ 13) 7.6.1 RDTIME RDCNTID ┌ 14) GRLEN 32 ┌
1.04	1) 2.2.1.6 32 ┌ 2) 3 ņ ņ ┌ 3) 3.2.3.2 FFINT.{S/D}.L FTINT.L.{S/D}, 3.2.3.3 FTINT{RM/RP/RZ/RNE}.L.{S/D} ┌

1

1.1

LoongArch Reduced Instruction Set Computing RISC

load/store load/store

32 64 LA32 LA64 LA64

LA32 LA64

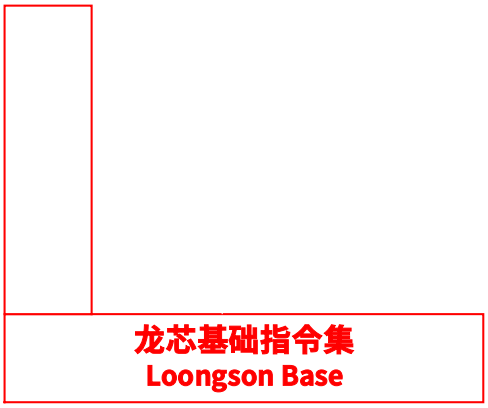
LA32 LA64

Loongson Base 1-1

Loongson Binary Translation LBT Loongson Virtualization LVZ

Loongson SIMD Extension LSX Loongson Advanced SIMD Extension

LASX



1-1

r

2 32

1.3

r 32 ɻ

r

r ŅF ņ

r

Ņ.XX ņ

r .B ɻ .H ɻ .W ɻ .BU ɻ .HU ɻ .WU

ɻ ɻ ɻ ɻ ɻ

r

ADD.W ADD.D BLT[U] BLT BLTU

ADD[I].{W/D} ADD.W ¡ ADD.D ¡ ADDI.W ADDI.D ┌

┌

1.4.2

32 Control and Status Register CSR

CSR ┌ CSR.%%%%.####

%%%% #### ┌ CSR.CRMD.PLV CRMD

PLV ┌

2

32

r r

2.1.2.1

Cache Cache ┌

Cache Cache Cache ┌

IBAR store

┌ Cache Cache code 8 9 CACOP

Hit Invalidate I-Cache Hit Invalidate and Writeback D-Cache ┌

2.1.8

4 ADEF ┌

┌

[1] ALE ┌

2.1.9

32 Weakly Consistency WC ┌

┌

dž<

2.2

2.2.1

2.2.1.1 ADD.W, SUB.W

```
add.w    rd, rj, rk
sub.w    rd, rj, rk
```

ADD.W rj rk [31:0] rd

r

ADD.W:

SUB.W rj rk [31:0] rd

r

SUB.W:

r

2.2.1.2 ADDI.W

```
addi.w    rd, rj, si12
```

ADDI.W rj 12 si12 32

rd r

ADDI.W:

r

2.2.1.3 LU12I.W

```
lu12i.w    rd, si20
```

LU12I.W 20 si20 12 0 rd r

LU12I.W:

ORI 12 r

2.2.1.4 SLT[U]

slt rd, rj, rk

sltu rd, rj, rk

SLT rj rk

rd 1 0 r

SLT:

SLTU rj rk

rd 1 0 r

SLTU:

SLT SLTU r

2.2.1.5 SLT[U]I

slti rd, rj, si12

sltui rd, rj, si12

SLTI rj 12 si12

rd 1 0 r

SLTI:

SLTUI rj 12 si12

rd 1 0 r

SLTUI:

SLTI SLTUI r

SLTUI r

2.2.1.6 PCADDU12I

pcaddu12i rd, si20

PCADDU12I 20 si20 12 0 PC

rd r

PCADDU12I:

r

2.2.1.7 AND, OR, NOR, XOR

and rd, rj, rk

or rd, rj, rk

nor rd, rj, rk

xor rd, rj, rk

AND rj rk

rd r

AND:

OR rj rk rd

r

OR:

NOR rj rk

rd r

NOR:

XOR rj rk

MUL.W rj rk [31:0]

rd r

MUL.W:

MULH.W rj rk [63:32]

rd r

MULH.WU rj rk

[63:32] rd r

MULH.WU:

2.2.1.11 DIV.W[U], MOD.W[U]

div.w rd, rj, rk

mod.w rd, rj, rk

div.wu rd, rj, rk

mod.wu rd, rj, rk

DIV.W DIV.WU rj rk rd

r

DIV.W:

DIV.WU:

MOD.W MOD.WU rj rk

rd ┌

MOD.W:

MOD.WU:

DIV.W MOD.W ┌ DIV.WU MOD.WU

┌

/ DIV.W/MOD.W DIV.WU/MOD.WU

┌

0 ┌

2.2.2

2.2.2.1 SLL.W, SRL.W, SRA.W

```
sll.w    rd, rj, rk
srl.w    rd, rj, rk
sra.w    rd, rj, rk
```

SLL.W rj rd ┌

SLL.W:

SRL.W rj rd ┌

SRL.W:

SRA.W rj rd ┌

SRA.W:

rk [4:0] r

2.2.2.2 SLLI.W, SRLI.W, SRAI.W

```
slli.w    rd, rj, ui5
srli.w    rd, rj, ui5
srai.w    rd, rj, ui5
```

SLLI.W rj rd r

SLLI.W:

SRLI.W rj rd r

SRLI.W:

SRAI.W rj rd r

SRAI.W:

5 ui5 r

2.2.3

2.2.3.1 BEQ, BNE, BLT[U], BGE[U]

```
beq     rj, rd, offs16
bne     rj, rd, offs16
blt     rj, rd, offs16
bge     rj, rd, offs16
bltu    rj, rd, offs16
bgeu    rj, rd, offs16
```

BEQ rj rd r

BEQ :

BNE rj rd r

BNE :

BLT rj rd

r

BLT :

BGE rj rd r

r

BGE :

BLTU rj rd

BLTU :

2

2.2.4

2.2.4.1 LD.{B[U]/H[U]/W}, ST.{B/H/W}

LD.{BU/HU } / rd ſ

LD.BU:

LD.HU:

ST.{B/H/W} rd

ST.B:

ST.H:

2.2.4.2 PRELD

preld hint, rj, si12

PRELD Cache Cache r rj
12 si12 r Cache r
PRELD hint Cache hint 0~31 32
r hint=0 load Cache hint=8 store Cache r hint
NOP r
PRELD Cache cached NOP
r
PRELD MMU r

2.2.5

2.2.5.1 LL.W, SC.W

ll.w rd, rj, si14
sc.w rd, rj, si14

LL.W SC.W N - - n r LL.W
rd SC.W
r LL.W LL

2.2.

2.2.6.1 DBAR

dbar hint

DBAR load/store r hint

r

hint 0 r load/store

Ņ DBAR 0” Ņ DBAR 0 ņ load/store

r

m(

2.2.7.3 RDCNTV{L/H}.W, RDCNTID

rdcntvl.w rd

rdcntvh.w rd

rdcntid rj

Counter 32 64 r

Stable Counter 0 1 1

3

32 r 32

IEEE 754-2008 r

r

0†ùŸ‰ð2 B±&ûGA¬å

r &ûGA

3-1 r

3-1

	E@CC-R+ ERTA-R+ ELTK-R+ ECHU-R+ EL@CC-R+ ELRTA-R+ EML@CC-R+ EMLRTA-R+ EL@W-R+ ELHM-R+ EL@W@-R+ ELHM@-R+ E@AR-R+ EMDF-R+ ERPQS-R+ EQDBHO-R+ EQRPQS-R+ EBNOXRHFM-R+ EBK@RR-R
	EBLO-bnmc-R
	EEHMS-R-V+ ESHMS-V-R+ ESHMSQL-V-R+ ESHMSQO-V-R+ ESHMSQY-V-R+ ESHMSQMD-V-R+
	ELNU-R+ ERDK+ LNUFQ1EQ-V+ LNUEQ1FQ-R+ LNUFQ1EBRQ+ LNUEBRQ1FQ+ LNUEQ1BE+ LNUBE1EQ+ LNUFQ1BE+ LNUBE1FQ
	ABDPY+ ABMDY
	EKC-R+ ERS-R R

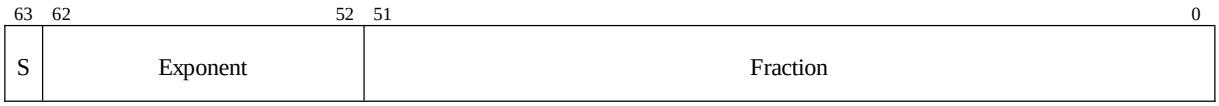
3.1

Dwonmdms	Eq`bshnm	R	ahsZ11\	U
		0		,1'015¥''/-Eq`bshnm(
Z0+ /wED\		/		*1'Dwonmdms,016(¥''0-Eq`bshnm(
		0		,1'Dwonmdms,016(¥''0-Eq`bshnm(
/wEE	</	/	/	''*Ÿ(
		0	/	'',Ÿ(
/wEE	</		/	'Rhfm`khmf Mns ` Mtladq+ RM`M(
			0	'Pthds Mns ` Mtladq+ PM`M(

£Ÿ ɻSNaN QNaN IEEE 754-2008 ɼ

3.1.1.2

64



S ɻExponent Fraction 3-3

3-3

Dwonmdms	Eq`bshnm	R	ahsZ40\	U
/	</	/	/	*/
		0	/	,/
/	</	/		*1'0/11¥''/-Eq`bshnm(
		0		,1'0/11¥''/-Eq`bshnm(
Z0+ /w6ED\		/		*1'Dwonmdms,0/12(¥''0-Eq`bshnm(
		0		,1'Dwonmdms,0/12(¥''0-Eq`bshnm(

fa ɻ fj fk fa fj fj fk ɼ

SNaN QNaN

SNaN 1 ɼ

1 ɼ

0 1 ɼ

ɻ SNaN QNaN QNaN ɼ

ɼ

QNaN QNaN ɼ

QNaN 0x7FC00000 QNaN 0x7FF8000000000000 ɼ

3.1.2

Word W 32b ɼ

ɼ

3.1.3

Floating-point Register FR ɻ

Condition Flag Register CFR Floating-point Control and Status Register FCSR ɼ

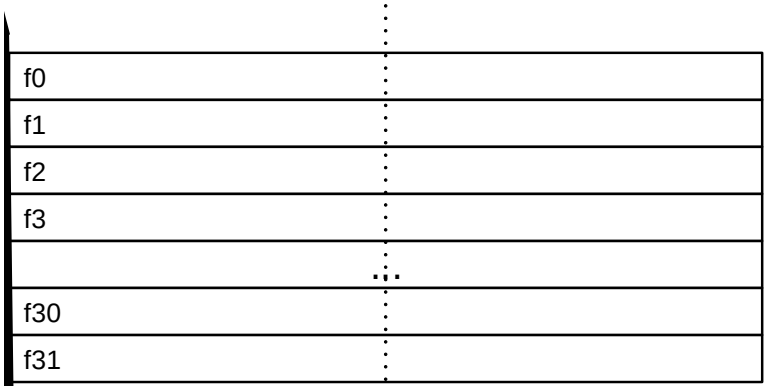
3.1.3.1

FR 32 f0~f31 ɼ

FR 32 ɼ FR 64 LA32 LA64 ɼ

32

FR ɼ



[31:0]

63 32

3.1.3.2

CFR 1 fcc0 CFR 1

1 0

3.1.3.3

FCSR 4 fcsr0~fcsr3 32 fcsr1~fcsr3 fcsr0
fcsr1~fcsr3 fcsr0 fcsr1~fcsr3 fcsr0
fcsr0 3-4

3-4 FCSR0

39/	Dm`akdr	QV	UYNTH 3 U 2 Y 1 N 0 T / H
694	/	Q/	/
897	QL	QV	3 / QMD HDDD 643,1//7 qntmcShdrSnDudm 0 QY HDDD 643,1//7 qntmcSnv`qcYdqn 1 QO HDDD 643,1//7 qntmcSnv`qcrOnrhshud 2 QL HDDD 643,1//7 qntmcSnv`qcrMdf`shud
0490/	/	Q/	/
1/905	Ek`fr	QV	Ek`fr UYNTH 1/ U 08 Y 07 N 06 T 05 H
12910	/	Q/	/
17913	B`trd	QV	UYNTH 17 U 16 Y 15 N 14 T 13 H
20918	/	Q/	/

FCSR1 FCSR0 Enables FCSR0
FCSR2 FCSR0 Cause Flags FCSR0
FCSR3 FCSR0 RM FCSR0

SR2

IEEE 754-2008

Inexact (I)

Underflow (U)

Overflow (O)

Division by Zero (Z)

Invalid Operation (V)

FCSR0 Cause r

FCSR0 Cause r

FCSR0 Enables r

r 1 Enable 1

Enable 0 FCSR0

Flag 1 r

r

r 3-5 r

3-5

H

QMD /+ ramnq l `k+ mnq l `k

£1,015 £1,0/11

QY /+ ramnq l `k

T QO /+ ramnq l `k+ mnq l `k

*1,015 *1,0/11

QL /+ ramnq l `k+ mnq l `k

,1,015 ,1,0/11

QMD * Ÿ , Ÿ

QY

N QO æ p

r

QNaN r

2 ķ (Z)

0 r

r

r

3.1.4.3 (O)

r

r

r

3.1.4.4 (U)

r

r

0

(-2^Emin, 2^Emin) r Emin

3.2

3.2.1

3.2.1.1 F{ADD/SUB/MUL/DIV}.{S/D}

fadd.s	fd, fj, fk	fadd.d	fd, fj, fk
fsub.s	fd, fj, fk	fsub.d	fd, fj, fk
fmul.s	fd, fj, fk	fmul.d	fd, fj, fk
fdiv.s	fd, fj, fk	fdiv.d	fd, fj, fk

FADD.{S/D} fj / fk / / fd r IEEE 754-2008 addition(x,y) r

FADD.S:

FADD.D:

FSUB.{S/D} fj / fk / / fd r IEEE 754-2008 subtraction(x,y) r

FSUB.S:

FSUB.D:

FMUL.{S/D} fj / fk / / fd r IEEE 754-2008 multiplication(x,y) r

FMUL.S:

FMUL.D:

FDIV.{S/D} fj / fk / / fd r IEEE 754-2008 division(x,y) r

FDIV.S:

FDIV.D:

3.2.1.2 F{MADD/MSUB/NMADD/NMSUB}.{S/D}

fmadd.s	fd, fj, fk, fa	fmadd.d	fd, fj, fk, fa
fmsub.s	fd, fj, fk, fa	fmsub.d	fd, fj, fk, fa
fnmadd.s	fd, fj, fk, fa	fnmadd.d	fd, fj, fk, fa
fnmsub.s	fd, fj, fk, fa	fnmsub.d	fd, fj, fk, fa

FMADD.{S/D} fj / fk /
fa / /
fd ┌

FMADD.S:

FMADD.D:

FMSUB.{S/D} fj / fk /
fa / /
fd ┌

FMSUB.S:

FMSUB.D:

FNMADD.{S/D} fj / fk /
fa / /
fd ┌

FNMADD.S:

FNMADD.D:

FNMSUB.{S/D}	fj	/		fk	/

FMINA.{S/D} fj / fk /

fd r IEEE 754-2008 minNumMag(x,y)

r

FMINA.S:

FMINA.D:

3.2.1.5 F{ABS/NEG}.{S/D}

fabs.s fd, fj fabs.d fd, fj

fneg.s fd, fj fneg.d fd, fj

FABS.{S/D} fj / 0

fd r

FABS.S:

-

B

[redacted]

FRECIP.{S/D} fj 1.0

/

RM`M	PM`M	mdf`shud u`ktd				onrhshud u`ktd			
		Ÿ	mnq l `k	rtamnq l `k	/	Ÿ	mnq l `k	rtamnq l `k	/

1 r

IEEE-754-2008 class(x) r

FCLASS.S:

FCLASS.D:

3.2.2

3.2.2.1 FCMP.cond.{S/D}

fcmp.cond.s cc, fj, fk fcmp.cond.d cc, fj, fk

cc r cond 22

r

bnmc		Sqtd Bnmchshnm	PM`M	HDDD 643,1//7
B@E	/w/			
BTM	/w7	TM		bnlo`qdPthdsTmnqcdqdc
BDP	/w3	DP		bnlo`qdPthdsDpt`k
BTDP	/wB			

3.2

3.2.3.1 FCVT.S.D, FCVT.D.S

fcvt.s.d fd, fj fcvt.d.s fd, fj

FCVT.S.D fj

fd r

FCVT.S.D:

7)

FCVT.D.S fj m" ı

fd r

FCVT.D.S:

) 5>I G

IEEE 754-2008 convertFormat(x) r

3.2.3.2 FFINT.{S/D}.{W/L}, FTINT.{W/L}.{S/D}

ffint.s.w	fd, fj	ftint.w.s	fd, fj
ffint.s.l	fd, fj	ftint.l.s	fd, fj
ffint.d.w	fd, fj	ftint.w.d	fd, fj
ffint.d.l	fd, fj	ftint.l.d	fd, fj

FFINT.{S/D}.{W/L} <o?º*Å*Y fj / /

/ f Þ:e G Ď

/ fd , Ṇ ṇ ɾ

FTINTRP.W.S:

FTINTRP.W.D:

FTINTRP.L.S:

FTINTRP.L.D:

FTINTRZ.{W/L}.{S/D} fj / /

/ fd Ṇ ṇ ɾ

FTINTRZ.W.S:

FTINTRZ.W.D:

FTINTRZ.L.S:

FTINTRZ.L.D:

FTINTRNE.{W/L}.{S/D} fj / /

/ fd Ṇ ṇ ɾ

FTINTRNE.W.S:

FTINTRNE.W.D:

FTINTRNE.L.S:

FTINTRNE.L.D:

IEEE 754-2008 ɾ

	HDDD 643,1//7
ESHMSQMD-zV.K|-zR.C|	bnmudqsSnHmsdfdqDw`bsShdrSnDudm'w(
ESHMSQY-zV.K|-zR.C|	bnmudqsSnHmsdfdqDw`bsSnv`qcYdqn'w(
ESHMSQO-zV.K|-zR.C|	bnmudqsSnHmsdfdqDw`bsSnv`qcOnrhshud'w(
ESHMSQL-zV.K|-zR.C|	bnmudqsSnHmsdfdqDw`bsSnv`qcMdf`shud'w(

3.2.4

3.2.4.1 FMOV.{S/D}

fmov.s fd, fj fmov.d fd, fj

FMOV.{S/D} fj / fd fj

/ r

FMOV.S

FMOV.d

IEEE 754 Cause Flags

r

3.2.4.2 FSEL

fsel fd, fj, fk, ca

FSEL r FSEL ca 0 fj

fd fk fd r

FSEL

3.2.4.3 MOVGR2FR.W, MOVGR2FRH.W

movgr2fr.w fd, rj

movgr2frh.w fd, rj

MOVGR2FR.W rj fd 32 r 64 fd

32 r

MOVGR2FR.W

MOVGR2FRH.W rj fd 32 fd 32 r

MOVGR2FRH.W

3.2.4.4 MOVFR2GR.S, MOVFRH2GR.S

movfr2gr.s rd, fj

movfrh2gr.s rd, fj

MOVFR2GR/MOVFRH2GR.S fj 32 / 32 rd ┌

MOVFR2GR.S

MOVFRH2GR.S

3.2.4.5 MOVGR2FCSR, MOVFCSR2GR

movgr2fcsr fcsr, rj

movfcsr2gr rd, fcsr

MOVGR2FCSR rj fcsr ┌

MOVGR2FCSR FCSR0 Cause Enables 1 FCSR1 Enables ┘ FCSR2 Cause Cause Enables 1 MOVGR2FCSR

┌

MOVGR2FCSR

MOVFCSR2GR fcsr 32 rd ┌

MOVFCSR2GR

fcsr ┌

3.2.4.6 MOVFR2CF, MOVCF2FR

movfr2cf cd, fj

movcf2fr fd, cj

MOVFR2CF fj cd ┌

MOVFR2CF

MOVCF2FR cj fd fd 0 ┌

MOVCF2FR

2 MOVGR2CF, MOVCF2GR

movgr2cf cd, rj

movcf2gr rd, cj

MOVGR2CF rj cd r

MOVGR2CF

MOVCF2GR cj rd rd 0 r

MOVCF2GR

3.2.5

3.2.5.1 BCEQZ, BCNEZ

bceqz cj, offs21

bcnez cj, offs21

BCEQZ cj 0 r

BCNEZ cj 0 C r

21 offs21 2

PC r

j b

3.2.6

3.2.6.1 FLD.{S/D}, FST.{S/D}

fld.s fd, rj, si12

4.2.2 Cache

4.2.2

NE 1 ｒ

TLB

4.2.3.5 INVTLB

invtlb op, rj, rk

INVTLB TLB TLB r

op 5 r

rj [9:0] ASID Ņ ASID”

0 r op ASID rj r0 r

rk Ņ VA ņ r op

rk r0 r

op op r

no	
/w/	r
/w0	r no</ r
/w1	F<0 r
/w2	F</ r
/w3	F</ @RHC @RHC r
/w4	F</ @RHC @RHC U@ U@ r
/w5	F<0 @RHC @RHC U@ U@ r

4.2.4

4.2.4.1 ERTN

ertn

ERTN r

PPLV ɻ PIE CSR.CRMD ERA r

PPLV ɻ PIE CSR.PRMD ERA CSR.ERA r

ERTN CSR.LLBCTL KLO 1 LLbit 0 LLbit r

4.2.4.2 IDLE

idle level

IDLE r

IDLE r

G) 1

store store TLB V=0

r

TLB V=0

r

TLB V=1

r CSR.CRMD.PLV

PLV r

store TLB V=1

D 0 r

5.4.3.2 TLB

TLB TLB ɻ ɻ ɻ TLB ɻ

r 4.2.3 r

5.4.3.3 TLB CSR

TLB CSR TLB

TLB r

BADV

TLBEHI

TLBELO0

TLBELO1

TLBIDX

ASID

PGDL

PGDH

PGD

TLBRENTRY

CSR TLB 7.4 CSR r

5.4.3.4 TLB

32 TLB Ņ INVTLB 0, r0, r0”

r

5.4.4 TLB

TLB r

```
# va:
# mem_type:          FETCH          LOAD    load      STORE    store
# plv                CSR.CRMD.PLV
# pa:
# mat:
# VALEN:
# PALEN:
# TLB[]: TLB[N]    TLB     N
# TLB_ENTRIES: TLB

#       TLB
```

#

TLB

#

6

6.1

6.1.1

32 r 12 1
IPI 1 TI 8 HWI0~HWI7 2 SWI0~SWI1 r
r
CSR.ESTAT.IS[12] r
r 0
r CSR.ESTAT.IS[11] r
CSR.TICLR TI 1 r
r 8 HWI[7:0]
CSR.ESTAT.IS[9:2] r
CSR CSR.ESTAT.IS[1:0] 1
0 r
CSR.ESTAT.IS Int Number r SWI0 0
SWI1 1 ň ň IPI 12 r

6.1.2

r IPI
TI ň ň SWI0 r

6.1.3

r 6.2.1 r

6.1.4

CSR.ESTAT.IS CSR.ECFG.LIE
int_vec r CSR.CRMD.IE=1 int_vec 0

6.2.3

6.2

6.2.1

TLB CSR.TLBRENTRY

CSR.EENTRY CSR.ESTA

Ecode IS

6.2.2

TLB

(ALE) > TLB [1]

6.2.3

CSR.CRMD PLV IE CSR.PRMD PPLV PIE CSR.CRMD PLV

0 IE 0

PC CSR.ERA

ERTN

CSR.PRMD PPLV PIE CSR.CRMD PLV IE

CSR.ERA

CSR.PRMD PPLV

PIE CSR.PRMD

[1] TLB TLB

6.3

r r

PC 0x1C000000 r MMU

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7.1

7-1

/w/		BQLC
/w0		OQLC
/w1		DTDM
/w3		DBEF
/w4		DRS@S
/w5		DQ@
/w6		A@CU
/wb		DDMSQX
/w0/	SKA	SKAHCW
/w00	SKA	SKADGH
/w01	SKA /	SKADKN/
/w02	SKA 0	SKADKN0
/w07		@RHC
/w08		OFCK
/w0@		OFCG
/w0A		OFC
/w1/		BOTHC
/w2/}/w22		R@UD/}R@UD2
/w3/		SHC
/w30		SBEF
/w31		SU@K
/w33		SHBKQ
/w5/	KKAhs	KKABSK
/w77	SKA	SKAQDMSQX
/w87		BS@F
/w07/}/w070		CLV/}CLV0

7.2

7.2.1

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RW—— ɻ ŗ

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R—— ŗ ŗ

R0—— 0 ŗ CSR

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W1—— 1 ŗ 0 0 ŗ

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CSR CSR

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CSRWR CSRXCHG rd

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7.4

7.4.1 CRMD

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7.4.2 PRMD

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7-3

09/	OOKU	QV	BRQ-BQLC OKU r 0 DQSM BRQ-BQLC OKU r _
1	OHD	QV	BRQ-BQLC HD r DQSM BRQ-BQLC HD r
2092	/	Q/	r / r

7.4.3 EUEN

r

r r

r

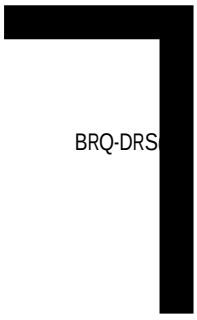
7-4

/	EOD	QV	r / 2-1 EOC r
2090	/	Q/	r / r

7.4.4 ECFG

r

7-5



r BRQ-DRS HRZ89/\ 0/

89/ KHDZ89/\ QV

8 r

hcd	Drt cd		
/wB		AQJ	
/wC	/	HMD	
/wD	/	HOD	
/wE	/	EOC	
/w01	/	EOD	
/w0@, /w2D			
/w2E	/	SKAQ	SKA

7.4.6 ERA

PC r

7-8

209/	OB	QV	OB r

7.4.7 BADV

r

TLB

ADEF PC

ALE

load PIL

store PIS

PIF

PME

1 L

7.4.8 EENTRY

TLB

1	JKN	QV	DQSM KKAhs r 0 DQSM KKAhs / / r JKN 0 DQSM r
2092	/	Q/	r / r

7.5

7.5.1 TLB TLBIDX

TLB TLB r 7-14 Inde/ n

019/	/	Q	/ r
20902	UOOM	QV	SKAQC SKA UOOM r SKARQBG SKA UOOM SKAVQ SKAEHKK SKA UOOM r SKA ɻkn`c ɻrsnqd ɻ ɻ Z20902\ r

7.5.3 TLB TLBELO0, TLBELO1

TLBELO0 TLBELO1 TLB TLB r
32 TLB TLB
TLBELO0 TLBELO1 rTLBELO0 TLBELO1
7-16 r
TLBWR TLBFILL TLB G ɻPPN0 ɻV0 ɻPLV0 ɻMAT0 ɻD0 ɻPPN1 ɻV1 ɻPLV1 ɻMAT1 ɻ D1 TLBELO0 TLBELO1 r
TLBRD TLB TLBELO0 TLBELO1
r

7-16 TLB

/	U	QV	U r
0	C	QV	C r
291	OKU	QV	OKU r
493	L@S	QV	L@S r
5	F	QV	F r SKAEHKK SKAVQ SKADKN/ SKADKN0 F 0 SKA F 0 r SKAQC SKA F 0 SKADKN/ SKADKN0 F 0 r
6	/	Q	/ r
O@KDM,497	OOM	QV	OOM r
209O@KDM,3	/	Q	/ r O@KDM<25 r

7.5.4 ASID

TLB ASID ┌ ASID

ASID ┌

7-17

7.5.7 PGD

r

CSR r

7-20

009/	/	Q	/ r
20901	A`rd	Q	BRQ-A@CU / BRQ-0FCK A`rd BRQ-0FCG A`rd r

7.5.8 TLB TLBRENTRY

TLB r TLB

r

7-21 TLB

49/	/	Q	SKA Z49/\ r / r
2095	O@	QV	SKA Z2095\ r r

7.5.9 DMW0~DMW1

r 5.2.1 r

7-22

/	OKU/	QV	0 OKU/ r
190	/	Q/	r / r
2	OKU2	QV	0 OKU2 r
493	L@S	QV	r
1395	/	Q/	r / r
16914	ORDF	QV	Z20918\ r
17	/	Q/	r / r
20918	URDF	QV	Z20918\ r

7.6.4 TICLR

annkd`m

ahs

hmsdfdq

ahsr'M(M

YdqnDwsdmc'____+M(M

RhfmDwsdmc'____+M(M

hrRM`M'____(  rhfm`khmf M`M 4ù ڑ ڀ v

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8.2.1

8.2.2

8.2.3

8.2.4

8.2.5

8.2.6

8.2.7

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMIN.D	fd, fj, fk	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0		fk				fj						fd		
FMAXA.S	fd, fj, fk	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1		fk				fj						fd		
FMAXA.D	fd, fj, fk	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0		fk				fj						fd		
FMINA.S	fd, fj, fk	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1		fk				fj						fd		
FMINA.D	fd, fj, fk	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0		fk				fj						fd		
FCOPYSIGN.S	fd, fj, fk	0	0	0	0	0	0	0	1	0	0	0	1	0																			

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FTINT.W.S	fd, fj	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	0	0	0	0	0	1			fj					fd		
FTINT.W.D	fd, fj	0	0	0	0	0	0	0	1	0	0	0	1	1	0	1	1	0	0	0	0	1	0			fj					fd		
FFINT.S.W	fd, fj	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	0	0	0	1	0	0			fj					fd		
FFINT.D.W	fd, fj	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	1	0	0	1	0	0	0			fj					fd		
SLTI	rd, rj, si12	0	0	0	0	0	0	1	0	0	0	si12														rj					rd		
SLTUI	rd, rj, si12	0	0	0	0	0	0	1	0	0	1	si12														rj					rd		
ADDI.W	rd, rj, si12	0	0	0	0	0	0	1	0	1	0	si12														rj					rd		
ANDI	rd, rj, ui12	0	0	0	0	0	0	1	1	0	1	ui12														rj					rd		
ORI	rd, rj, ui12	0	0	0	0	0	0	1	1	1	0	ui12														rj					rd		
XORI	rd, rj, ui12	0	0	0	0	0	0	1	1	1	1	ui12														rj					rd		
CSRRD	rd, csr	0	0	0	0	0	1	0	0	csr												0	0	0	0	0					rd		
CSRWR	rd, csr	0	0	0	0	0	1	0	0	csr												0	0	0	0	1					rd		
CSRXCHG	rd, rj, csr	0	0	0	0	0	1	0	0	csr												rj!=0,1									rd		
CACOP	code, rj, si12	0	0	0	0	0	1	1	0	0	0	si12														rj					code		
TLBSRCH		0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0
TLBRD		0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
TLBWR		0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
TLBFILL		0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
ERTN		0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
IDLE	level	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	1								level							
INVTLB	op, rj, rk	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	1	1			rk					rj					op		
FMADD.S	fd, fj, fk, fa	0	0	0	0	1	0	0	0	0	0	0	1			fa					fk					fj					fd		
FMADD.D	fd, fj, fk, fa	0	0	0	0	1	0	0	0	0	0	1	0			fa					fk					fj					fd		
FMSUB.S	fd, fj, fk, fa	0	0	0	0	1	0	0	0	0	1	0	1			fa					fk					fj					fd		
FMSUB.D	fd, fj, fk, fa	0	0	0	0	1	0	0	0	0	1	1	0			fa					fk					fj					fd		
FNMADD.S	fd, fj, fk, fa	0	0	0	0	1	0	0	0	1	0	0	1			fa					fk					fj					fd		
FNMADD.D	fd, fj, fk, fa	0	0	0	0	1	0	0	0	1	0	1	0			fa					fk					fj					fd		
FNMSUB.S	fd, fj, fk, fa	0	0	0	0	1	0	0	0	1	1	0	1			fa					fk					fj					fd		
FNMSUB.D	fd, fj, fk, fa	0	0	0	0																												

		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ST.W	rd, rj, si12	0 0 1 0 1 0 0 1 1 0 si12 rj rd
LD.BU	rd, rj, si12	0 0 1 0 1 0 1 0 0 0 si12 rj rd
LD.HU	rd, rj, si12	0 0 1 0 1 0 1 0 0 1 si12 rj rd
PRELD	hint, rj, si12	0 0 1 0 1 0 1 0 1 1 si12 rj hint
FLD.S	fd, rj, si12	0 0 1 0 1 0 1 1 0 0 si12 rj fd
FST.S	[illegible]	0 0 1 0 1 0 1 1 0 1 si12 rj fd
FLD.D	fd, rj, si12	0 0 1 0 1 0 1 1 1 0 si12 rj fd
FST.D	fd, rj, si12	0 0 1 0 1 0 1 1 1 1 si12 rj fd
DBAR	hint	0 0 1 1 1 0 0 0 0 1 1 1 0 0 1 0 0 hint
IBAR	hint	0 0 1 1 1 0 0 0 0 1 1 1 0 0 1 0